et al. ('551); claims 6-9, 17, 24, 25, 34, and 35 stand rejected under § 103(a) as unpatentable over Matsumoto; claims 11-14, 18, 36, and 40 stand rejected under § 103(a) as unpatentable over Matsumoto in view of Kunii et al. ('493); claim 10 stands rejected under § 103(a) as unpatentable over Matsumoto in view of Dohjo et al.; claim 15 stands rejected under § 103(a) as unpatentable over Matsumoto in view of Kunii et al. and Dohjo et al.; and, claim 39 stands rejected under § 103(a) as unpatentable over Matsumoto in view of Iizuka ('268A). Theses rejections are respectfully traversed at least for the reasons provided below.

With respect to Matsumoto applied in the § 102(e) rejection and the § 103(a) rejections as the primary reference, Applicants respectfully submit that Matsumoto teaches forming gate electrodes corresponding to the channel regions, as disclosed in col. 3, lines 23-26, and col. 4, lines 60-66, and that there is no discussion, suggestion, or inference of lightly doped regions being overlapped with the gate electrode.

Although the Examiner relied upon Fig. 1 of Matsumoto for showing the claimed limitation that the lightly doped regions are overlapped with the gate electrode, Applicants respectfully submit that Matsumoto is silent regarding this feature. As Matsumoto only explicitly teaches to form the gate electrode as corresponding to the channel regions, and as there is no disclosure, teaching, or suggestion of the lightly doped regions are overlapped with the gate electrode, the Examiner's reliance on Fig. 1 of Matsumoto is improper.

Moreover, as it is not clear whether Matsumoto intentionally drafted Fig. 1, or other Figures for that matter, to show the lightly doped regions overlapping with the gate electrode or not, the Examiner appears to rely on for what appears to be the impreciseness of drawing Fig. 1 to deduce Applicants' claimed feature without any support in the specification of the Matsumoto reference for the alleged disclosure of lightly doped regions being overlapped with the gate electrode in Fig. 1.

In addition, claim 11 recites an additional limitation that a distance between the channel forming region and the pair of first regions in the first thin transistor is different from that of the second thin film transistor. The Examiner stated that it was well known in the art at the time of invention that active matrix pixel TFTs were susceptible to charge leakage. Applicants respectfully note that the Examiner is relying upon Kunii for this statement, particularly, column 13, lines 46-48. Further, Applicants respectfully submit that the reliance on Kunii is not proper, since this teaching is directed to the variation of the LDD lengths within a single TFT.

As Matsumoto is defective and does not teach, disclose, or suggest lightly doped regions overlapping with the gate electrode recited in Applicants' pending claims, and as none of the secondary references cures this deficiency, the application of Matsumoto, separately or in combination with other secondary cited prior art references, is improper.

In view of the arguments set forth above, Applicants respectfully request reconsideration and withdrawal of the § 102(e) rejection and the § 103(a) rejections.

CONCLUSION

Having responded to all rejections set forth in the outstanding final Office Action, it is submitted that claims 1-25 and 34-41 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

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